REMARKS

This response is to the Final Office Action mailed on November 15, 2006. Claims 1-10 and 12-19 are pending in this action. Claims 9-10 and 12-18 are allowed. Claims 1–8 and 19 are rejected. Claim 19 is cancelled herein without prejudice.

Applicant acknowledges the change in Examiner.

Allowed Claims

Claims 9-10 and 12-18 are allowed. Applicant acknowledges and thanks the Examiner for recognition of the allowable condition of these Claims. Applicant notes that Claim 9 was amended in response to the first Office Action, and that the amended claim listing of page 2 of the Final Office Action was a typographical error.

Claim rejections under 35 U.S.C. §102

Claims 1-3 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Jigour (U.S. Patent No. 5,991,194). In the Office Action, Jigour is cited as disclosing: a serial flash memory; and a programmable logic device having an interface coupled to the serial flash memory, wherein the interface is configured to identify the serial flash memory, wherein the serial flash memory operates in accordance with the serial peripheral interface (SPI) protocol, and wherein the serial flash memory is coupled to the interface by a standard SPI four-wire interface, as is claimed in the present application. Applicant respectfully disagrees with this reading of Jigour.

As Examiner states, Jigour does disclose a system comprising; a serial flash memory and an interface coupled to the serial flash memory, wherein the flash memory is accessible through a four-pin Serial Peripheral Interface (SPI) bus. However, Jigour does not disclose a "programmable logic device having an interface coupled to the serial flash memory."

A "programmable logic device" (PLD), as the term is used by practitioners of ordinary skill in the applicable art, is generally used to denote a family of semiconductor devices that includes, for example, Field Programmable Gate Arrays (FPGAs). (See, e.g., Applicant's Related Art section, paragraph [0002]). As is well-known in the art, such devices share the characteristic of being internally configurable

to perform various logical tasks. This differs, for example, from merely being able to execute a set of instructions held in a memory. A "programmable, non-volatile memory array," such as Jigour discloses (column 4 lines 26–35) is not a "programmable logic device." Jigour does not disclose a "programmable logic device," and the Office Action does not cite any element of Jigour as a "programmable logic device."

For anticipation to be determined under 35 U.S.C. §102, the cited reference must teach every aspect of the claimed invention, either explicitly or impliedly. Any feature not directly taught must be inherently present. Jigour does not teach every aspect of Applicant's invention. Jigour does not teach, either directly or indirectly, Applicant's claim of "a serial flash memory; and a programmable logic device having an interface coupled to the serial flash memory, wherein the interface is configured to identify the serial flash memory."

Applicant respectfully submits, therefore, that Claims 1–3 are not anticipated under 35 U.S.C. §102 by the teachings of Jigour. Claims 1–3 of the present application are, therefore, in condition for allowance as originally presented.

Claim rejections under 35 U.S.C. §103

Applicant notes that the reference to DeCaro is a typographical artifact of the First Office Action, and acknowledges Examiners' statement that argument in response is persuasive and that DeCaro is no longer cited as prior art under 35 U.S.C. §103.

In the present Office Action Claims 4–8 are rejected under 35 U.S.C. §103 as being unpatentable over Jigour in view of Office Notice of a "well-known feature." Claim 19 is also "rejected for the same reasons as stated above with respect to Claims 4–8." The well known feature, of which notice is taken, is having a start address register to provide a start address to the flash memory. Applicant acknowledges the Office Notice and also acknowledges Examiner's citation of the prior art references.

Claims 4–8, however, are dependent from, and include further limitations to, Claim 1. As Claim 1 is allowable, Claims 4–8 are also allowable. Applicant

respectfully requests allowance of Claims 4–8 for at least the same reasons as stated above with respect to Claims 1–3. Claims 1–3 are not anticipated by Jigour. Therefore, Claims 4–8 are not anticipated by Jigour in view of Office Notice.

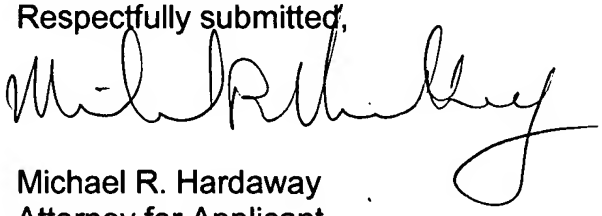
Claim 19 is also allowable for at least the reasons stated above. However, in the interest of expediting allowance of the present application, Applicant requests cancellation of Claim 19 without prejudice.

CONCLUSION

All remaining claims are now in condition for allowance and a Notice of Allowance is respectfully requested.

If there are any questions, Applicant's attorney can be reached at Tel: 408-879-6149.

Respectfully submitted,



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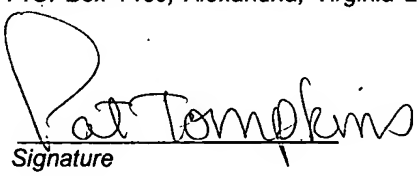
*I hereby certify that this correspondence is being deposited with the United States Postal Service as **first class mail** in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450, on January 10, 2007.*

Pat Tompkins
Name



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